WHAT IS CLAIMED IS:

1. A nonvolatile memory apparatus comprising:

a plurality of terminals including a first terminal, a second terminal and other terminal; and

a nonvolatile memory array including a plurality of nonvolatile memory cells,

wherein said first terminal receives a clock signal,

wherein said second terminal receives information for specifying an arbitrary one of operations which include a read operation and a program operation,

wherein each of said nonvolatile memory cells stores multi-bit type data having more than two bits,

wherein in said read operation, said nonvolatile memory apparatus reads multi-bit type data from ones of said nonvolatile memory cells, converts multi-bit type data to binary type data, and outputs binary type data to outside via said other terminal not said command terminal in response to said clock signal, and

wherein in said program operation, said nonvolatile memory apparatus receives binary type data from outside via said other terminal except said command terminal in response to said clock signal, converts binary type data to multi-bit type data, and writes multi-bit type data to ones of said nonvolatile memory cells.

2. A nonvolatile memory apparatus according to claim 1, wherein each of said memory cells stores multi-bit type data as a threshold voltage

within one of a plurality of threshold voltage ranges,

wherein one of said threshold voltage ranges is a threshold voltage range indicating an erase state and others of said threshold voltage ranges are threshold voltage ranges indicating programming states, and

wherein said nonvolatile memory apparatus controls moving threshold voltages of said ones of nonvolatile memory cells to within one of threshold voltage ranges according to multi-bit type data in said program operation.

3. A nonvolatile memory apparatus according to claim 2, wherein said operations further include an erase operation, and

wherein said nonvolatile memory apparatus controls moving threshold voltages of said ones of nonvolatile memory cells to within said threshold voltage range indicating said erase state in said erase operation.

4. A nonvolatile memory apparatus according to claim 3, further comprising:

a circuit,

wherein in said read operation, said circuit senses a status of data according to a threshold voltage of said nonvolatile memory cell which is within said threshold voltage range indicating said erase state or within said threshold voltage range indicating said program state.

5. A nonvolatile memory apparatus according to claim 4, wherein said other terminal is a third terminal,

wherein said third terminal receives binary type data in response to

said clock signal, and

wherein said third terminal outputs binary type data in response to said clock signal.

6. A nonvolatile memory apparatus comprising:

a control circuit;

a plurality of terminals including a first terminal, a second terminal and an other terminal; and

a nonvolatile memory array including a plurality of nonvolatile memory cells,

wherein said first terminal is capable of receiving a clock signal,

wherein said second terminal is capable of receiving information for specifying arbitrarily any one of operations which include a read operation and a program operation,

wherein each of said nonvolatile memory cells is capable of storing multi bit type data being more than two bits,

wherein said control circuit executes operation steps corresponding to specified operation read out from a program memory,

wherein in said read operation, said control circuit controls, based on operation steps corresponding to said read operation, reading of multi bit type data from ones of said nonvolatile memory cells, converting multi bit type data to binary type data, and outputting binary type data via said other terminal except said command terminal in response to said clock signal, and

wherein in said program operation, said control circuit controls, based on operation steps corresponding to said program operation, receiving of

binary type data via said other terminal except said command terminal in response to said clock signal, converting binary type data to multi bit type data, and writing multi bit type data to ones of said nonvolatile memory cells.

7. A nonvolatile memory apparatus according to claim 6, wherein each of said memory cells stores multi bit type data as a threshold voltage within one of a plurality of threshold voltage ranges,

wherein one of said threshold voltage ranges is indicating an erase state and others of said threshold voltage ranges are indicating programming states, and

wherein said control circuit controls moving threshold voltage of said ones of a nonvolatile memory cells to within one of threshold voltage ranges according to multi bit type data in said operation steps corresponding to said program operation.

8. A nonvolatile memory apparatus according to claim 7, wherein said operations include an erase operation, and

wherein in said erase operation, said control circuit controls, based on operation steps corresponding to said erase operation, moving of threshold voltage of said ones of nonvolatile memory cells to within threshold voltage range indicating said erase state.

9. A nonvolatile memory apparatus according to claim 8, wherein said control circuit comprises:

a circuit,

wherein in said read operation, said circuit senses status of data according to threshold voltage of said nonvolatile memory cell which is within said voltage of said nonvolatile memory cell which is within said threshold voltage range indicating said erase state or within said threshold voltage range indicating said program state.

10. A nonvolatile memory apparatus according to claim 9, wherein said other terminal is a third terminal,

wherein in said program operation, said third terminal is capable of receiving binary type data in response to said clock signal, and

wherein in said read operation, said third terminal is capable of outputting binary type data in response to said clock signal.

11. A nonvolatile memory apparatus according to claim 6, wherein said control circuit includes said program memory therein.